CSIRO Intelligent Grid Research Cluster - Project 7

Control Strategies to ensure efficient, reliable and economic operation of the micro-grid.

Microgrid Operation and Control

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DELIVERABLE 3: Converter Control

1. Introduction

Power electronics dc-ac converters are either current source type or voltage source type. Current source inverters (or converters) convert dc current to ac voltages, while voltage source converters convert dc voltages into ac voltages. Many of the distributed generators (DGs), like solar photovoltaic (PV) cells, fuel cells, produce dc voltages. Others, like wind, tidal, produce ac voltages with varied frequency and cannot be directly connected to the grid. Their output voltages are therefore rectified to produce dc voltages, which are converted ac voltages by the converter. Therefore voltage source converters are commonly used for grid connection of DGs.

In this report, we shall investigate the structure and control of voltage source converters (VSCs). A VSC, being a switched device, can introduce harmonics in the system due the switching of the power semiconductor switches. To suppress these harmonics, passive filter circuits are used. The design of the filter circuits will also be discussed in this report. While designing a switching controller, the dynamics of the filter circuit must be considered. We shall discuss a generalized control structure which can perform simultaneous voltage and current control. This generalized control structure can also be used for either current or voltage control.

2. Voltage Source Converter Structure

A single-phase full bridge VSC that is supplying an RL load is shown in Fig. 1. This is often called an H-bridge, since this resembles the eighth letter of the English alphabet. The converter dc side (often called the dc bus) is supplied by a voltage source V_{dc}. The converter contains four switches S_1 to S_4. Each switch consists of a power semiconductor device (e.g., IGBT, MOSFET) and anti-parallel diode that maintains the continuity of current once the switch turns off (see the in-set). The switches in each leg are complementary, i.e., when S_1 is on, S_4 is off and vice versa. This prevents switches short circuiting the dc source. When the switches S_1 and S_2 are on, the voltage source is connected across the point *AB*, and the current *i* builds up in the positive direction. Alternatively when the switches S_3 and S_4 are on, the voltage source is connected across the point *BA*, and the current *i* builds up in the negative direction. The main idea of switching control is to control the switches such are a desired current is tracked or a desired voltage is produced across the terminals *AB*.

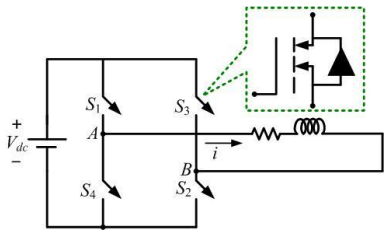

Fig. 1. An H-bridge VSC.

The schematic diagram of a three-phase full bridge converter is shown in Fig. 2. This contains six switches S_1 to S_6, each consisting of a power semiconductor device and an anti-parallel diode. Like in the case of the H-bridge converter, the switches of each leg are complementary (e.g., when S_1 is on, S_4 is off). This is most common form of three-phase converter available, where the dc bus voltage is equal to V_{dc}. However, this has the disadvantage that the algebraic sum of the three output

currents must be zero, i.e., $i_a + i_b + i_c = 0$. This is a disadvantage if the converter is required to supply unbalanced load. Alternatively, three more converter structures can be used, in which, any of the phases can be independently controlled.

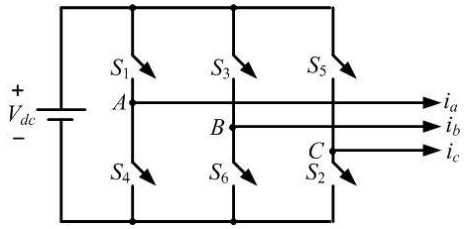

Fig. 2. A three-phase VSC.

The converter structure shown in Fig. 3, is essentially the same as shown in Fig. 2, except that the dc bus is split into two, with a center point *N*. The dc bus voltage is still equal to V_{dc}. But it now contains two dc sources, each equal to $V_{dc}/2$. The center point *N*, when connected to the load neutral, provides a path for the unbalanced (zero-sequence) components to flow. Hence, the three legs of the converter can be treated separately and we can control each leg independent of the other two legs [1].

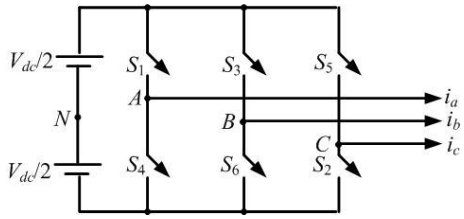

Fig. 3. A neutral-clamped three-phase VSC.

The four-leg VSC topology was first proposed in [1] and was subsequently used and analyzed in [2-3]. This is shown in Fig. 4, in which the center point 4th leg (n') is connected to the load neutral (n) through a resistor and an inductor. The current though this path is i_0 and this current is used to cancel the zero-sequence components of the load. In this case also, we can treat each individual phase separately.

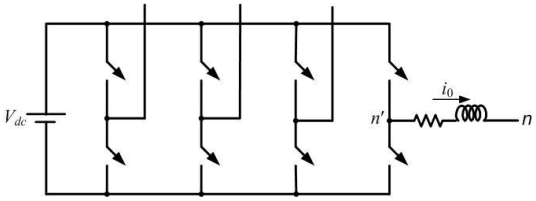

Fig. 4. A 4-leg VSC.

Alternatively, for high power applications, the VSC shown in Fig. 5 can be used. It contains three H-bridge converters that are connected to a common dc source [4-5]. The outputs of the VSCs are connected to three single-phase transformers. The secondary sides of the transformers are connected in wye, with the neutral point being connected to the load neutral *n*. The transformers provide voltage boosting, isolation and prevent the converter switches from shorting the dc bus. In this case also, we can treat each of the phases independently.

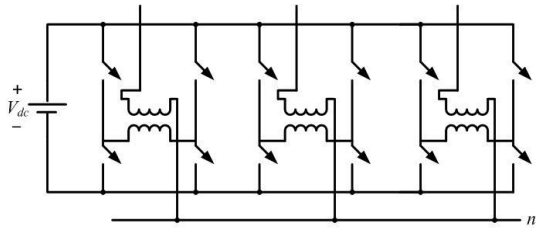

Fig. 5. VSC structure with three h-bridges and transformers.

A comparative study of these topologies for distribution system power quality conditioner is presented in [6]. For more details on converter topologies and their analysis, one can refer to [7].

3. Filter Structure

As have been mentioned in the previous section that each phase of the converters shown in Figs. 3-5 can be controlled independently. We shall therefore consider the converter control design of just one phase with the understanding that similar control law can also be derived for the other two phases. The single-phase equivalent circuit of a converter, with its associated filter, is shown in Fig. 6. Two types of filters are commonly used – inductance-capacitance (LC) and inductance-capacitance-inductance (LCL) filters. In Fig. 6, the filter inductors are denoted by L_1 and L_2, while the capacitor is denoted by C. The voltage across the capacitor is denoted by v_c. The resistances R_1 and R_2 are the associated with the inductances L_1 and L_2 respectively, arising due to their finite quality factor. The aim of the converter control is to generate the switching signal $u = \pm 1$. The converter control techniques with these two filters are discussed next.

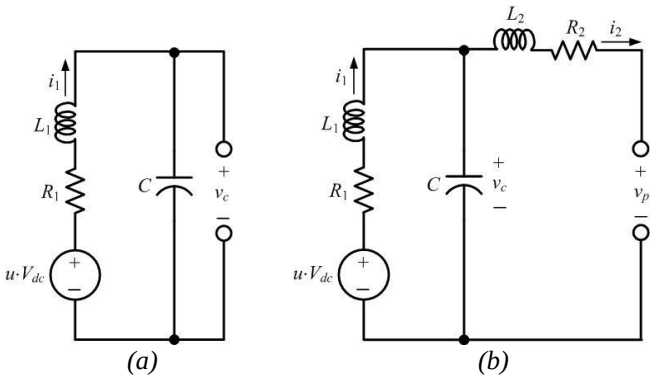

Fig. 6. Single-phase VSC equivalent circuit with (a) LC and (b) LCL filter.

4. Control of Converter with LC Filter

In this section, we shall discuss a voltage control strategy, for which the LC filter structure will be employed. We shall present a design example at the end, which will highlight the design process.

A. State Feedback Control

Defining a state vector as $x^T = [v_c \quad i_1]$, the state space equation of the system can be written from Fig. 6 (a) as

$$\dot{x} = Ax + Bu_c \tag{1}$$

where u_c is the feedback control law, based on which the converter switching signal $u = \pm 1$ is generated and the matrices A and B are

$$A = \begin{bmatrix} 0 & 1/C \\ -1/L_1 & -R_1/L_1 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ V_{dc}/L_1 \end{bmatrix}$$

There are various converter control strategies. However we shall adopt the linear quadratic regulator (LQR) based state feedback control. This was used in [8], where it was shown that hysteretic current control for such system can lead to an unstable operation. Assuming that the references for the states are available and are denoted by $x_{ref} = [v_{cref} \quad i_{1ref}]$, the state feedback control law is given as

$$u_c = -K(x - x_{ref}) \tag{2}$$

where $K = [k_1 \quad k_2]$ is the feedback gain matrix, which is computed based on LQR and design parameters. The schematic diagram of the control law is given in Fig. 7 (a).

The LC filter structure is most suitable for tracking the output voltage, where the voltage reference (v_{cref}) can be pre-specified. However, it is rather difficult to find a reference (i_{1ref}) for the converter output current i_1. One approach can be to set this reference to zero. This will however lead to incorrect control action. To avoid this problem, a state transformation has been used in [8]. This is however feasible only when the overall system structure and rough estimates of the system parameters are known a priori. Therefore this solution cannot be stated as a general solution. It should be noted that the current i_1 should only contain lower frequency components, while its high frequency components should be zero. Therefore, if we pass this current through a high-pass filter (HPF), then we expect the output (i_{1HPF}) of the filter to be zero. The HPF structure is given by

$$\frac{i_{1HPF}}{i_1} = \frac{s}{s + \alpha} \tag{3}$$

where α determines the cutoff frequency of the filter.

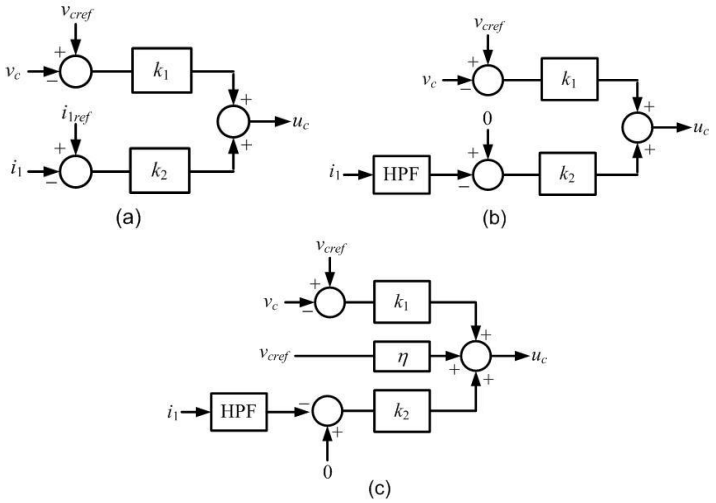

Fig. 7. Three different feedback control structures: (a) full state feedback, (b) partial state feedback with high-pass filter and (c) partial state feedback with feed forward control.

It may also be desirable to use a feed forward of the voltage reference in order to obtain better tracking characteristics. This is shown in Fig. 7 (c), where the reference voltage is multiplied by a constant η and is added to the feedback signals. In any of the control schemes, the converter switching pulses are obtained from the computed values of u_c. This is discussed in the next section.

B. Pulse Width Modulated (PWM) Control

For the control of the VSC, we shall use a bi-polar switching strategy [7]. This is shown in Fig. 8. This consists of a triangular carrier waveform (v_{tri}), which varies from – 1 to + 1 with a duty ratio of 0.5 (Fig. 8 a). The control output is sampled twice in each cycle, one at the negative peak of the carrier waveform and once at the positive peak. The sampler is assumed to be an impulse modulator that consists of a train of pulses as shown in Fig. 8 (a). The control signal (u_c) is shown in Fig. 8 (c). The control signal is sampled by the sampler of Fig. b (b) and is held by a zero order hold (ZOH) circuit. The output u_c^* of the ZOH is shown in Fig. 8 (d), while its inverse ($-u_c^*$) is shown in Fig. 8 (e).

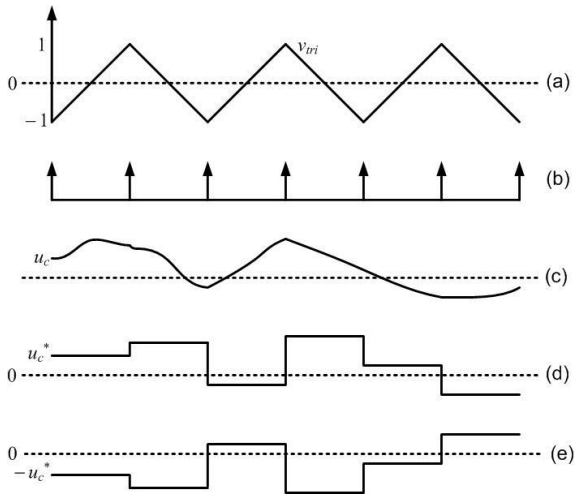

Fig. 8. PWM switching control: (a) carrier waveform, (b) sampler pulse train, (c) the control signal (d) sampled and ZOH output and (d) negative of the sampled and ZOH output.

The switching pulses ($u = \pm 1$) is generated by comparing u_c^* and $-u_c^*$ with the carrier waveform (v_{tri}). With respect to Fig. 1 for a single-phase inverter, the algorithm is given by

$$\begin{aligned}
&\text{If } u_c^* > v_{tri} \text{ then } S_1 \text{ is ON} \\
&\text{elseif } u_c^* < v_{tri} \text{ then } S_1 \text{ is OFF} \\
&\text{If } u_c^* < v_{tri} \text{ then } S_4 \text{ is ON} \\
&\text{elseif } u_c^* > v_{tri} \text{ then } S_4 \text{ is OFF}
\end{aligned} \tag{4}$$

$$\begin{aligned}
&\text{If } -u_c^* > v_{tri} \text{ then } S_3 \text{ is ON} \\
&\text{elseif } -u_c^* < v_{tri} \text{ then } S_3 \text{ is OFF} \\
&\text{If } -u_c^* < v_{tri} \text{ then } S_2 \text{ is ON} \\
&\text{elseif } -u_c^* > v_{tri} \text{ then } S_2 \text{ is OFF}
\end{aligned} \tag{5}$$

It can be seen from (4) that operations of the switches S_1 and S_4 are complementary. Similarly, it is evident from (5) that S_3 and S_2 operations are complementary. However, in order to prevent both the switches of a leg to be ON at a given time (shoot through fault), a small delay, called the blanking period, is introduced between the operations of two switches of the same leg. Most commercial inverters automatically introduce the blanking period. However this period is not considered for converter analysis.

C. Closed-Loop Converter Model

Ignoring delay, we can assume that the average over the switch period is obtained by a linear modulator as in [7]. The PWM amplifier can then be considered as an ideal unit gain amplifier, i.e., we can assume $u_c = u$. Under this condition, the open-loop is the same as given by (1). We now derive the closed-loop system model. Let us first consider the transfer function of the HPF, given by (3). This can be written as

$$i_{1HPF} = \left(\frac{s}{s+\alpha}\right) i_1 = \left(1 - \frac{\alpha}{s+\alpha}\right) i_1 = i_1 - i_{1LPF} \tag{6}$$

where i_{1LPF} is given by

$$i_{1LPF} = \left(\frac{\alpha}{s+\alpha}\right) i_1 \tag{7}$$

Equation (7) can be expressed in differential equation form as

$$\frac{d}{dt} i_{1LPF} = -\alpha\, i_{1LPF} + \alpha\, i_1 \tag{8}$$

Let us now define a new state vector as $x_e^T = [v_c \quad i_1 \quad i_{1LPF}]$. Then combining (1) with (8), we get an augmented state space equation of the form

$$\dot{x}_e = A_e x_e + B_e u_c \tag{9}$$

where

$$A_e = \begin{bmatrix} A & 0 \\ \alpha & -\alpha \end{bmatrix} \text{ and } B_e = \begin{bmatrix} B \\ 0 \end{bmatrix}$$

The discrete-time equivalent (9) is given as

$$x_e(k+1) = Fx_e(k) + Gu_c(k) \tag{10}$$

where k is time index and the matrices F and G are [9]

$$F = e^{A_e \Delta T}, \quad G = \int_0^{\Delta T} e^{A_e t} B_e dt, \quad \Delta T = \text{Samplig interval}$$

From Fig. 7 (c), the feedback control law is given by

$$u_c(k) = v_0 + k_1 v_{cref}(k) - k_1 v_c(k) - k_2 i_{1HPF}(k) \tag{11}$$

Substituting (6) in (11), we get

$$\begin{aligned} u_c(k) &= v_0 + k_1 v_{cref}(k) - k_1 v_c(k) - k_2 i_1(k) + k_2 i_{1LPF}(k) \\ &= -\begin{bmatrix} k_1 & k_2 & -k_2 \end{bmatrix} \bar{x}_e(k) + v_0 + k_1 v_{cref}(k) \end{aligned} \tag{12}$$

Combining (12) with (10), the closed-loop state equation is given by

$$x_e(k+1) = (A_e - B_e \begin{bmatrix} k_1 & k_2 & -k_2 \end{bmatrix} \bar{x}_e(k) + v_0 + k_1 B_e v_{cref}(k) \tag{13}$$

D. Numerical Examples

Let us consider the system shown in Fig. 9 in which the converter is connected with an RL plus back emf load. The system parameters used and their definition are given in Table 1. The frequency of the triangular waveform (v_{tri}) is taken as 15 kHZ and the sampling frequency is chosen twice of this frequency, i.e., 30 kHz. The frequency response of the open-loop system, which contains only the LC filter dynamics of (1), is shown in Fig. 10. It is obvious that the filter resonates around 2.2 kHz.

Table 1: System Parameters with LC filter

System Quantities	Parameter values
System frequency	50 Hz
Back emf (v_s)	230 V (rms)
Load resistance (R_s)	5 Ω
Load inductance (L_s)	11.6 mH
Filter capacitance (C)	25 μF
Filter inductance (L_1)	0.2 mH
Filter resistance (R_1)	0.1 Ω

DC voltage (V_{dc})	350 V

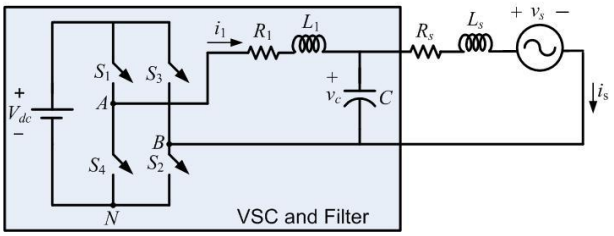

Fig. 9. H-bridge converter with LC filter connected to an RL plus back emf load.

The closed-loop frequency response, for various values of HPF coefficient α, is shown in Fig. 10. In this the input is the voltage reference v_{cref} and the output is the capacitor voltage v_c. It can be seen that a = 500, the circuit behaves like an ideal amplifier with a gain of 0 dB (i.e., $v_{cref} = v_c$) till around 3 kHz. The 3 dB cut-off frequency is around 6.5 kHz, indicating that the converter-filter system will track a voltage reference up to this frequency. The tracking error however increases as α increase. However, it is still less than 2 dB, indicating a maximum tracking error of 20%.

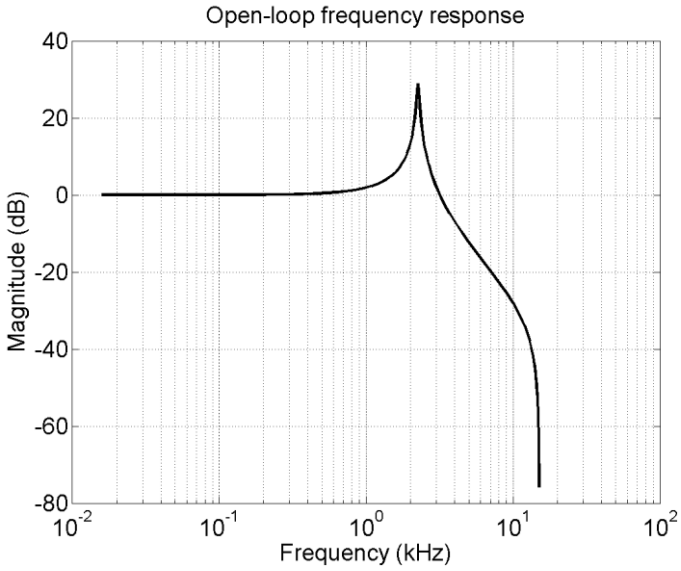

Fig. 10. Open-loop frequency response with LC filter.

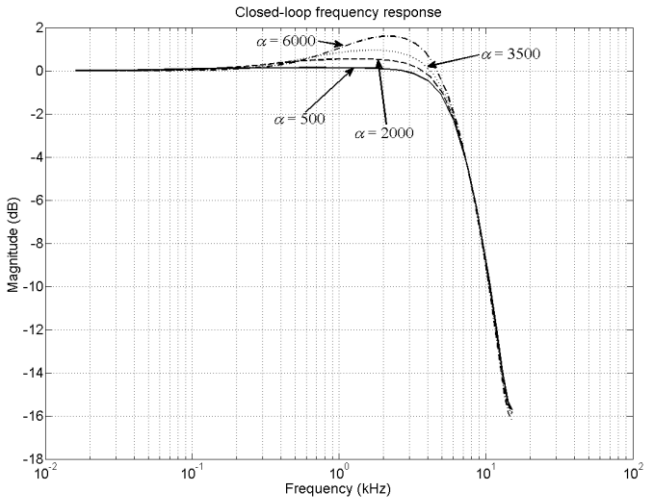

Fig. 11. Closed-loop frequency response for various values of α.

The phase of the closed-loop system, for two values of α, is shown in Fig. 12. It can be seen that the phase shift between the reference and output voltages is almost zero when the system frequency is 100 Hz or less. This implies that the converter is able to track a reference waveform of 50 Hz without any appreciable phase shift. However, the phase shift increases as the system frequency increases. Also note that the phase shift is more for lower values of α. From Figs. 11 and 12 it is evident that α = 500 is sufficient for tracking fundamental frequency (50 Hz) waveforms. However, for higher frequency tracking, this value has to chosen as a compromise between phase error and magnitude error.

The H-bridge converter switching behavior is shown in Fig. 13. The intersection of the sampled control signal u_c^* and its negative with the 15 kHz triangular waveform is shown in the top sub-plot. As evident from Fig. 9 and (4), the voltage (v_{AN}) across the first leg is generated from the intersection of u_c^* and v_{tri}. Similarly the voltage (v_{BN}) across the second leg is generated from the intersection of $-u_c^*$ and v_{tri}. The difference between v_{AN} and v_{BN} gives the converter output voltage, which can take on values of + V_{dc} (350 V), – V_{dc} (– 350 V) and 0 V. The converter leg and output voltages are also shown in Fig. 13.

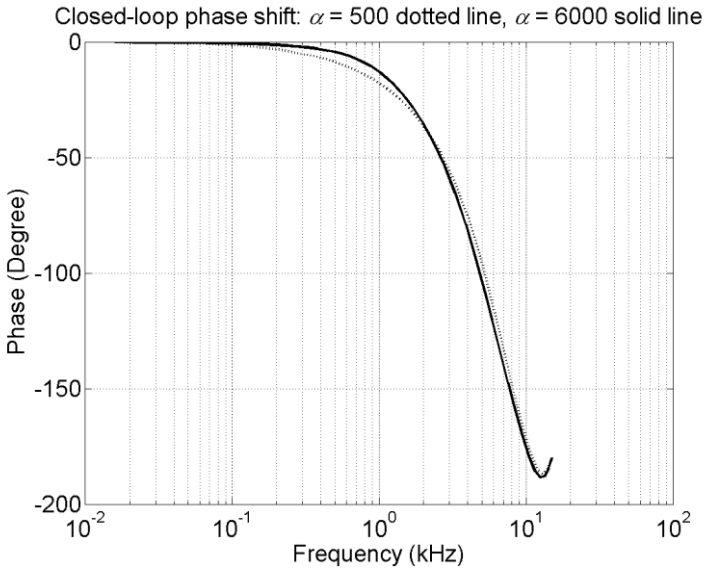

Fig. 12. Closed-loop phase shift for two values of α.

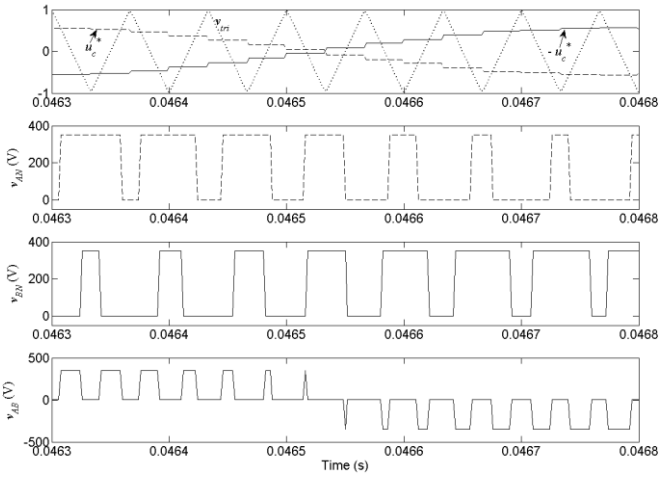

Fig. 13. H-bridge converter switching behavior.

To evaluate the performance of voltage tracking, we consider the system of Fig. 9, the data for which are given in Table 1. First we assume that the converter is required to track a 50 Hz voltage waveform with a peak of 230 V. The HPF coefficient is chosen as α = 500. The system performance is shown in Fig. 14. The reference and converter output voltages are shown in Fig. 14 (a). The error between these two voltages is shown in Fig. 14 (b). It can be seen that the peak of the tracking error is around 10 V. We now choose a reference voltage that contains odd harmonics, given by

$$v_{cref} = 150 \times \left[\sin(\omega t) + \frac{\sin(3\omega t)}{3} + \frac{\sin(5\omega t)}{5} + \frac{\sin(7\omega t)}{7} + \frac{\sin(9\omega t)}{9} + \frac{\sin(11\omega t)}{11} + \frac{\sin(13\omega t)}{13} + \frac{\sin(15\omega t)}{15} + \frac{\sin(17\omega t)}{17} + \frac{\sin(19\omega t)}{19} + 0.2\sin(31\omega t) \right]$$

The reference voltage waveform is shown in Fig. 15 (a). The voltage tracking error for an α of 500 is shown in Fig. 15 (b), while that for an α of 6000 is shown in Fig. 15 (c). It can be seen that the magnitude of the tracking error is considerably less when high filter coefficient is chosen, which reduces the phase error – the major contributor of the tracking error.

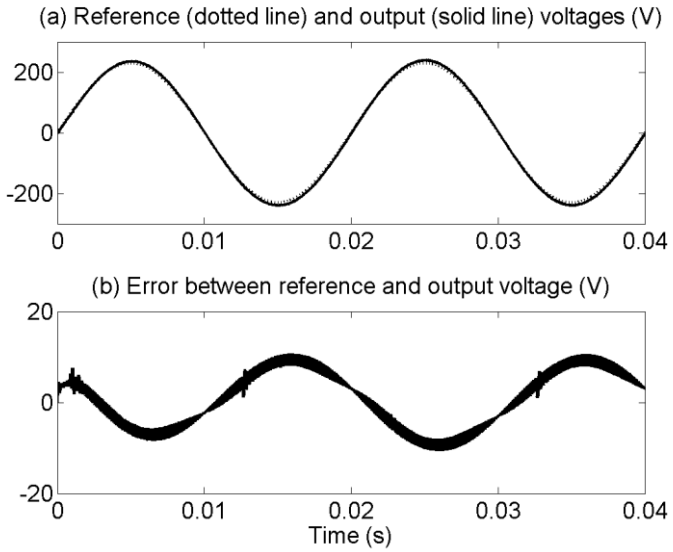

Fig. 14. Voltage tracking performance for a 50 Hz reference voltage.

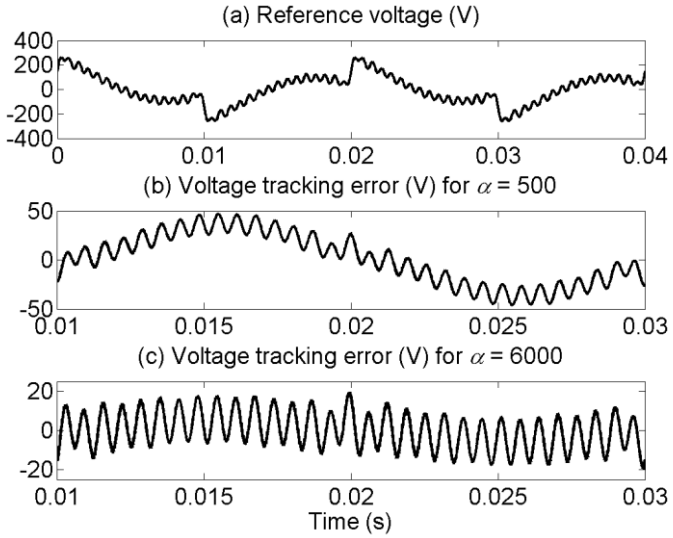

Fig. 15. Voltage tracking performance for a distorted reference voltage.

5. Control of Converter with LCL Filter

In this section, we shall highlight the control of converters with LCL filters. In particular, this structure is useful for current control, where the current to be injected is pre-specified.

A. Closed-loop Converter Model

The single-phase equivalent circuit of the converter with LCL filter is shown in Fig. 6 (b). With respect to this figure, we define a state vector as $x^T = [v_c \quad i_1 \quad i_2]$. The state space equation of the system can be written as

$$\dot{x} = Ax + Bu_c + Dv_p \tag{14}$$

$$A = \begin{bmatrix} 0 & 1/C & -1/C \\ -1/L_1 & -R_1/L_1 & 0 \\ 1/L_2 & 0 & -R_2/L_2 \end{bmatrix}, \quad B = \begin{bmatrix} 0 \\ V_{dc}/L_1 \\ 0 \end{bmatrix}, \quad D = \begin{bmatrix} 0 \\ 0 \\ -1/L_2 \end{bmatrix}$$

The purpose of the control is to track a reference current i_{2ref}. We shall therefore use two HPFs, one for i_1 and the other for v_c. The HPFs are derived in the same fashion as (6-8). They are

For i_1 with HPF-1:

$$i_{1HPF} = \left(\frac{s}{s+\alpha_1}\right) i_1 = \left(1 - \frac{\alpha_1}{s+\alpha_1}\right) i_1 = i_1 - i_{1LPF} \tag{15}$$

where i_{1LPF} is given by

$$i_{1LPF} = \left(\frac{\alpha_1}{s+\alpha_1}\right) i_1 \tag{16}$$

Equation (15) can be expressed in differential equation form as

$$\frac{d}{dt} i_{1LPF} = -\alpha_1 i_{1LPF} + \alpha_1 i_1 \tag{17}$$

For v_c with HPF-2:

$$v_{cHPF} = \left(\frac{s}{s+\alpha_2}\right) v_c = \left(1 - \frac{\alpha_2}{s+\alpha_2}\right) v_c = v_c - v_{cLPF} \tag{18}$$

where v_{cLPF} is given by

$$v_{cLPF} = \left(\frac{\alpha_2}{s+\alpha_2}\right) v_c \tag{19}$$

Equation (18) can be expressed in differential equation form as

$$\frac{d}{dt} v_{cLPF} = -\alpha_2 v_{cLPF} + \alpha_2 v_c \tag{20}$$

Let us now define a new state vector as $x_e^T = [v_c \quad i_1 \quad i_2 \quad v_{cLPF} \quad i_{1LPF}]$. Then combining (14), (17) and (20), we get an augmented state space equation of the form

$$\dot{x}_e = A_e x_e + B_e u_c + D_e v_p \tag{21}$$

where

$$A_e = \begin{bmatrix} A & \begin{matrix} 0 \\ 0 \end{matrix} \\ \begin{bmatrix} \alpha_2 & 0 & 0 \\ 0 & \alpha_1 & 0 \end{bmatrix} & \begin{bmatrix} -\alpha_2 & 0 \\ 0 & -\alpha_1 \end{bmatrix} \end{bmatrix}, \; B_e = \begin{bmatrix} B \\ 0 \\ 0 \end{bmatrix} \text{ and } \; D_e = \begin{bmatrix} C \\ 0 \\ 0 \end{bmatrix}$$

The closed-loop control scheme is shown in Fig. 16. From this figure, the control law is given as

$$\begin{aligned} u_c &= -k_1 v_{cHPF} - k_2 i_{1HPF} + k_3 (i_{2ref} - i_2) \\ &= -k_1 v_c + k_1 v_{cLPF} - k_2 i_1 + k_2 i_{1LPF} + k_3 (i_{2ref} - i_2) \\ &= -\begin{bmatrix} k_1 & k_2 & k_3 & -k_1 & -k_2 \end{bmatrix} \underline{x}_e + k_3 i_{2ref} \end{aligned} \tag{22}$$

Combining (19) and (20), the closed-loop state equation is given by

$$\dot{x}_e = (A_e - B_e \begin{bmatrix} k_1 & k_2 & k_3 & -k_1 & -k_2 \end{bmatrix}) \underline{x}_e + k_3 B_e i_{2ref} + D_e v_p \tag{23}$$

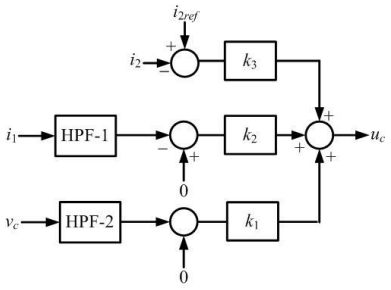

Fig. 16. The current control structure.

B. Numerical Examples

Let us consider the same system as given in Fig. 17. The system data are given in Table 2. Let us first assume that we have the full system knowledge (i.e., the knowledge of the load resistance and inductance). In this event, v_p becomes equal to v_s and the matrix A of (14) is altered to include the load resistance and inductance as

$$A = \begin{bmatrix} 0 & 1/C & -1/C \\ -1/L_1 & -R_1/L_1 & 0 \\ 1/(L_2 + L_s) & 0 & -(R_1 + R_2)/(L_2 + L_s) \end{bmatrix}$$

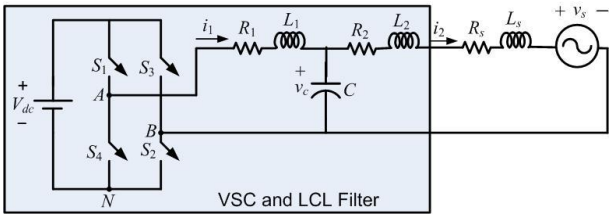

Fig. 17. H-bridge converter with LCL filter connected to an RL plus back emf load.

Table 2: System Parameters with LCL filter

System Quantities	Parameter values
System frequency	50 Hz
Back emf (v_s)	230 V (rms)
Load resistance (R_s)	5 Ω
Load inductance (L_s)	11.6 mH
Filter capacitance (C)	25 μF
Inside filter inductance (L_1)	0.2 mH
Inside filter resistance (R_1)	0.1 Ω
Outside filter inductance (L_2)	1.25 mH
Outside filter resistance (R_2)	0.1 Ω
DC voltage (V_{dc})	450 V
HPF-1 (α_1)	5000
HPF-2 (α_2)	5000

The controller gains, obtained with the full system knowledge, are

$$K = \begin{bmatrix} 2.6254 & 19.6589 & 2661 \end{bmatrix}$$

The closed-loop frequency response, as per (23), is shown in Fig. 18. It can be seen that the magnitude has a unit gain below 300 Hz and then it starts rolling off above 5 kHz. The system response while tracking a fundamental frequency waveform with a peak of 25 A is shown in Fig. 19 (a), while the tracking error is shown in Fig. 19 (b). It can be seen that tracking error, barring some distortion at the peaks of the waveform, is negligible. The distortions at the peaks can be minimized by increasing the dc bus voltage. This may however be not always possible.

The problem with the design mentioned above is that it is not possible to estimate the load or the back emf most of the time. We therefore have to design the controller based on the available filter data (i.e., through 23). From the LQR design, these gains are given as

$$K = \begin{bmatrix} 7.16 & 19.27 & 428.88 \end{bmatrix}$$

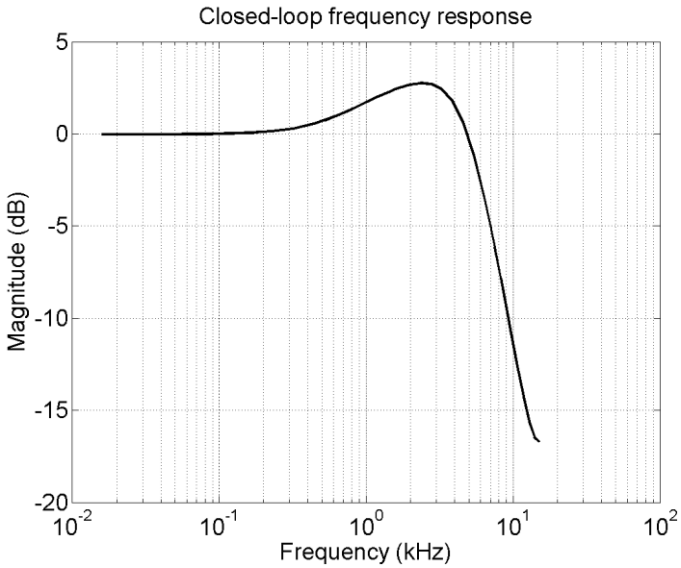

Fig. 18. Closed-loop frequency response with LCL filter.

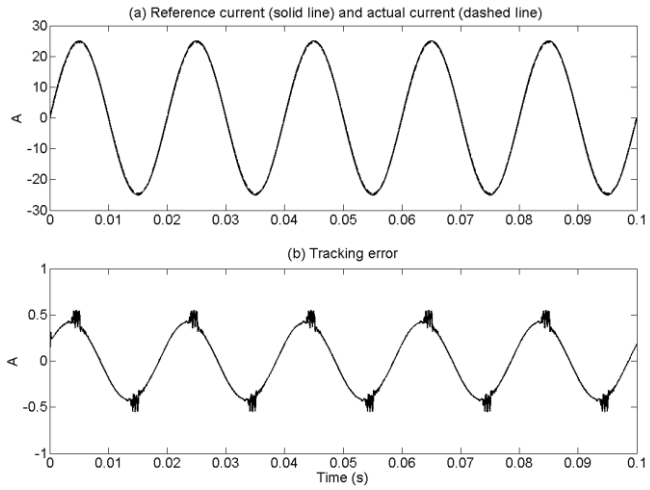

Fig. 19. Current tracking with full system knowledge.

We now know that the current will be injected in series with an equivalent circuit with a large enough inductor. Therefore in order to have a better current tracking, the output inductor gain is increased and the gains associated with the inner inductor and the filter capacitor are decreased. The controller gains are then modified to

$$K = \begin{bmatrix} 5 & 10 & 1000 \end{bmatrix}$$

The system tracking performance with the modified controller gains is shown in Fig. 20. Comparing with Fig. 19 it can be seen that the tracking error has increased. However, the since the peak error is below 1 A, the tracking performance is still adequate and acceptable. In general, a current tracking can work perfectly if the current flows through a low impedance path. However, when the current has to flow through a relatively large inductor, the controller has to work harder and may saturate. This problem is not associated with a voltage controller since it can have a direct

control over the capacitor voltage, especially since the capacitors are connected in shunt.

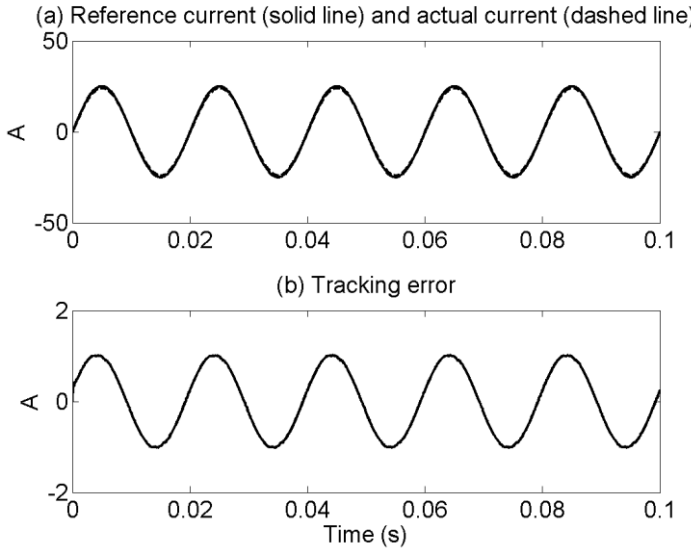

Fig. 20. Current tracking with incomplete system knowledge.

6. Conclusions

In this report, a method of converter control using PWM and state feedback is presented. Two different converter-filter structures are considered. Two separate controller design principles are presented, on for each filter structure. The relevant equations are derived for each of the controllers presented. The bandwidth issues of the filters are also discussed. From the presented results and discussion, it can be surmised that voltage controller has a better tracking performance than a current tracker. In this report we have only presented the single-phase performance of the converters, since most of the distributed energy resources (e.g., PV, plug-in electric vehicles etc) will be connected to the grid through such converters. However the analysis and design principles presented are general in nature and can be extended to include three-phase converters.

7. References

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